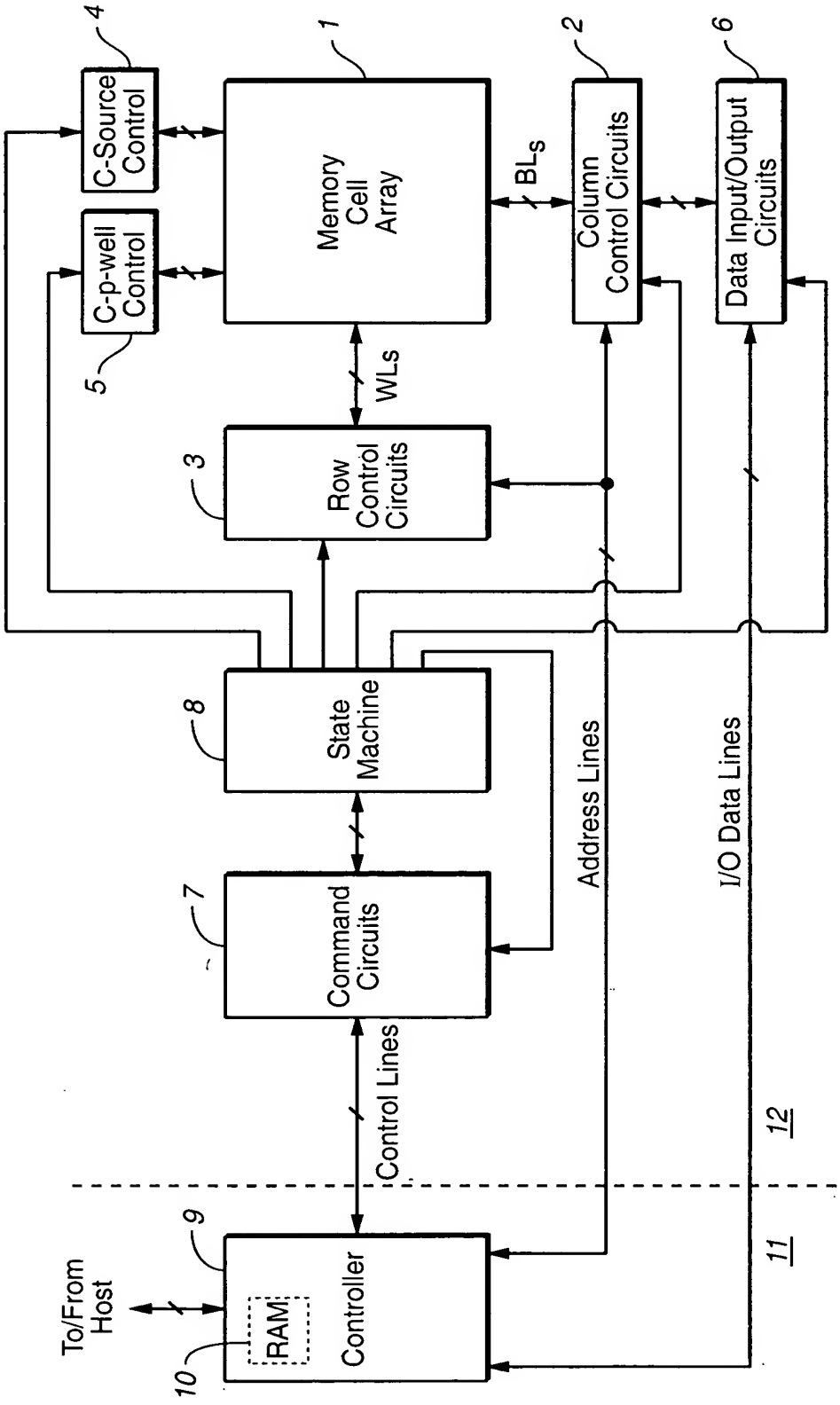

4
C-Source Control
1
Memory Cell Array
2
Column Control Circuits
6
Data Input/Output Circuits
BLs
C-p-well Control
5
WLs
3
Row Control Circuits
8
State Machine
7
Command Circuits
Address Lines
I/O Data Lines
Control Lines
12
11
9
To/From Host
RAM
Controller
10

FIG._1

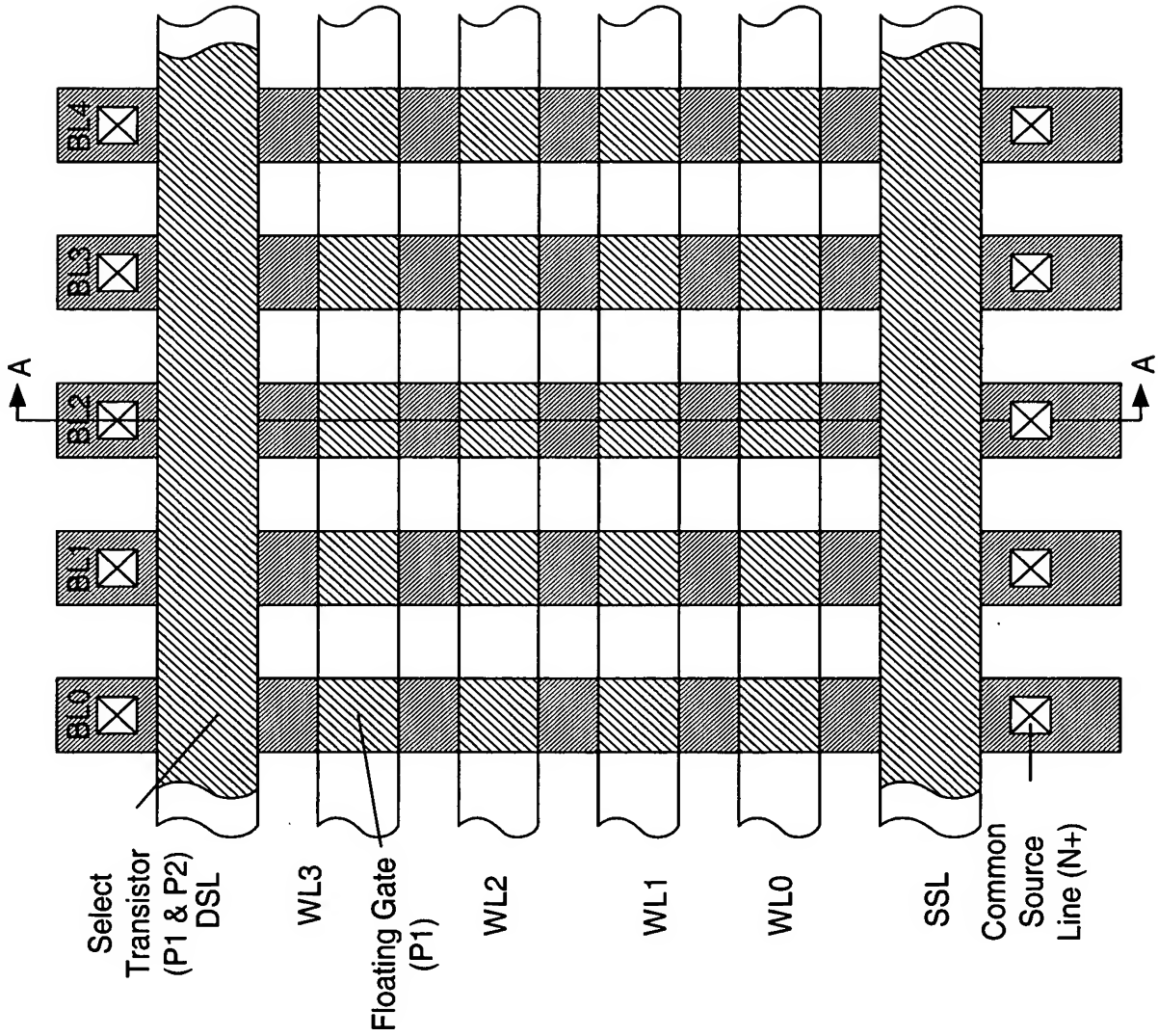



FIG._ 2A (PRIOR ART)

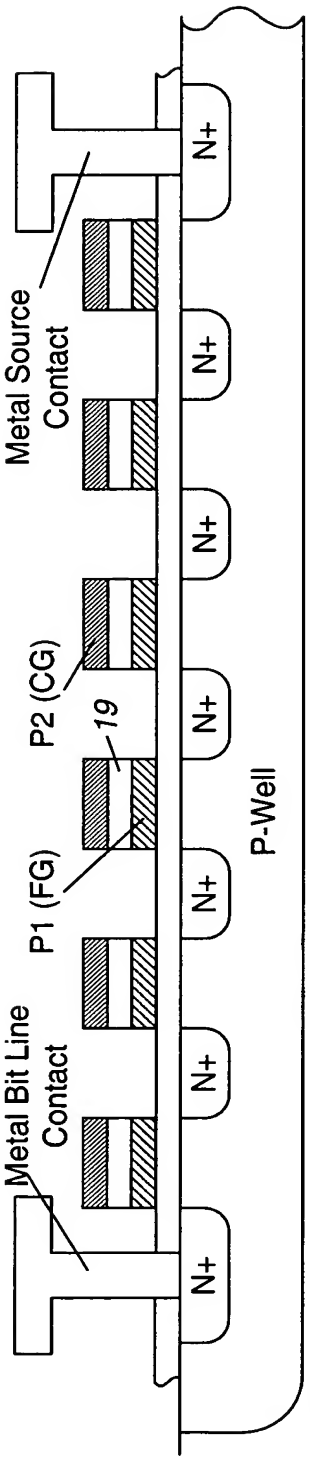



FIG._2B (PRIOR ART)
(Section A-A)

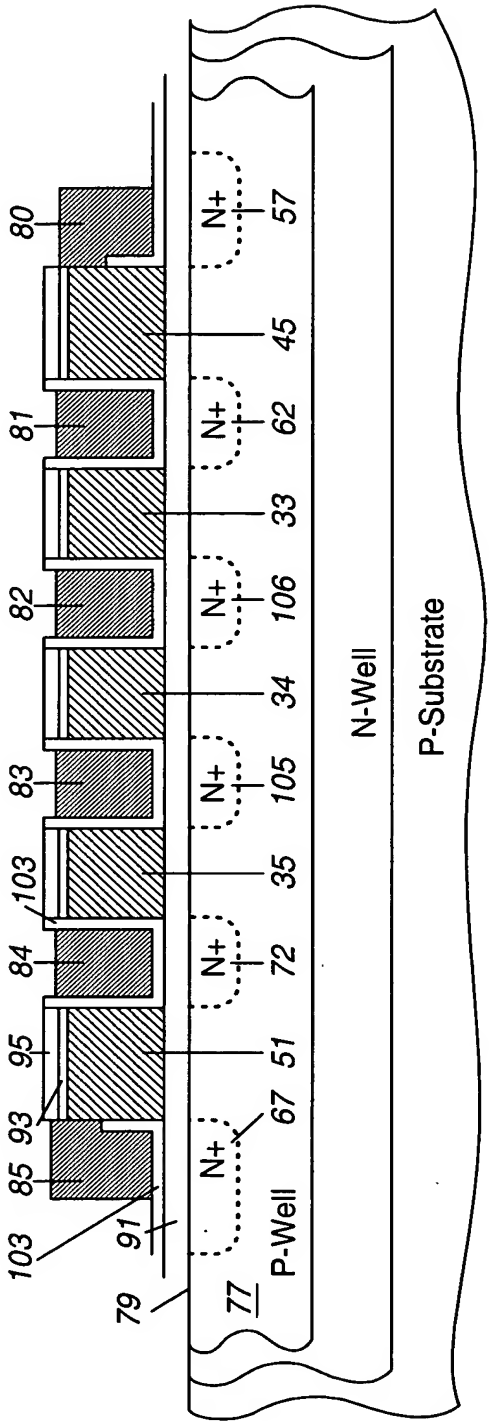



FIG._4
(Section A-A)

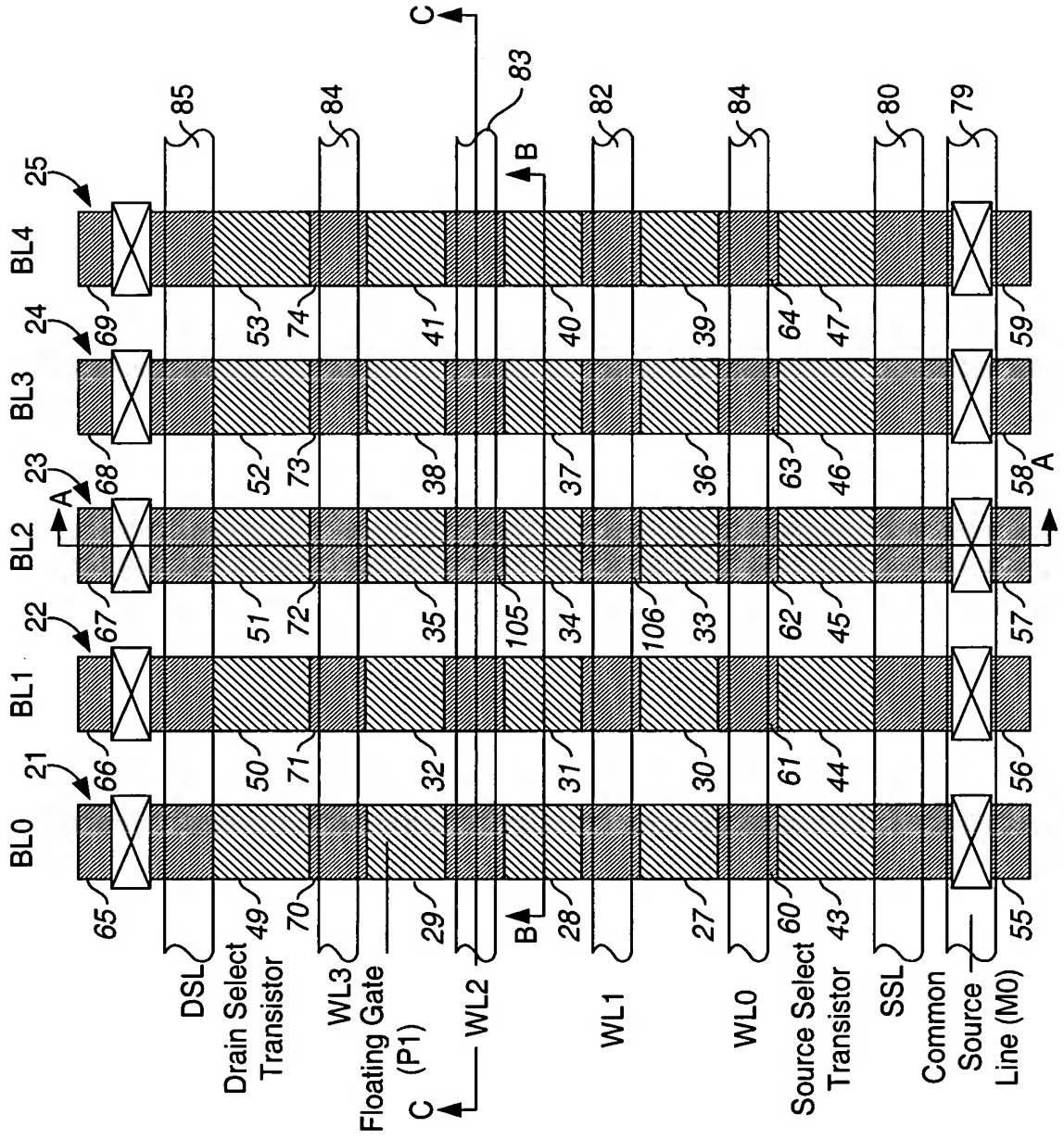

BL0
BL1
BL2
BL3
BL4
DSL
Drain Select Transistor
WL3
Floating Gate (P1)
WL2
WL1
WL0
Source Select Transistor
SSL
Common Source Line (M0)
A
B
C

FIG._3

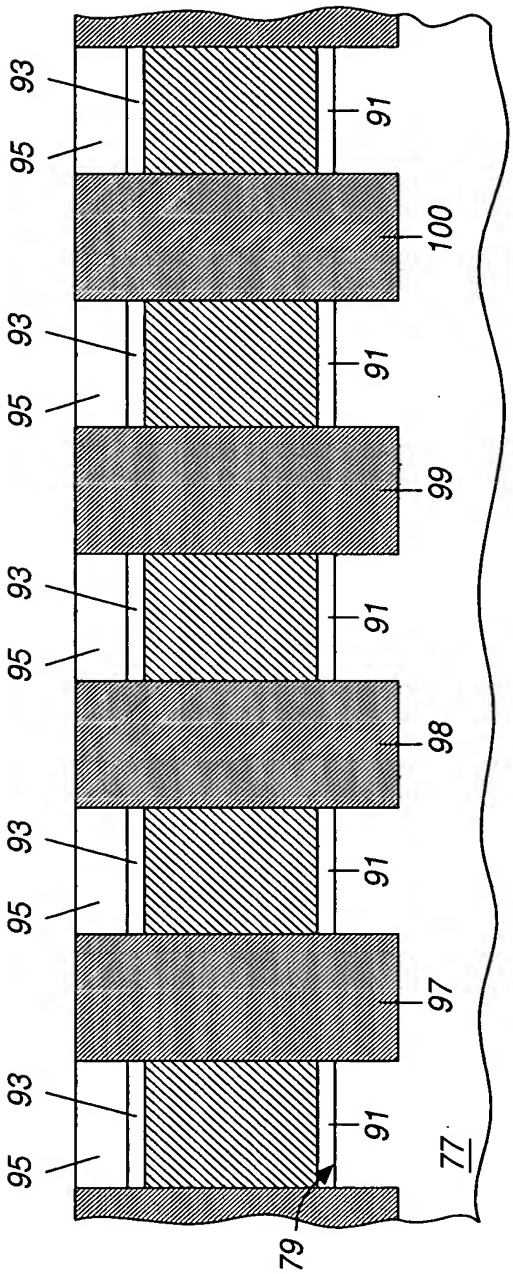



FIG._5A
(Section B-B)

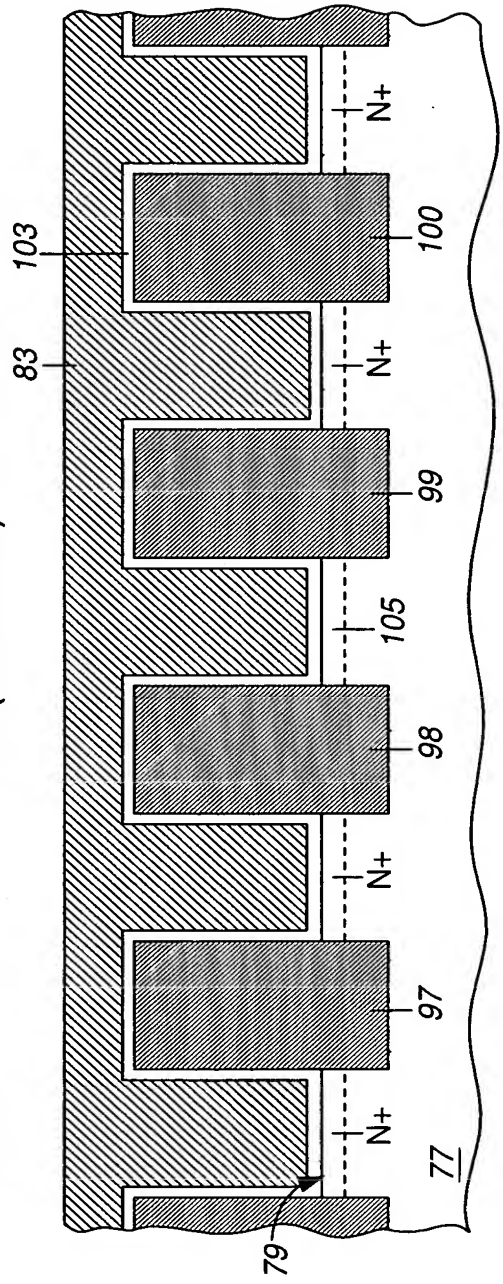



FIG._5B
(Section C-C)

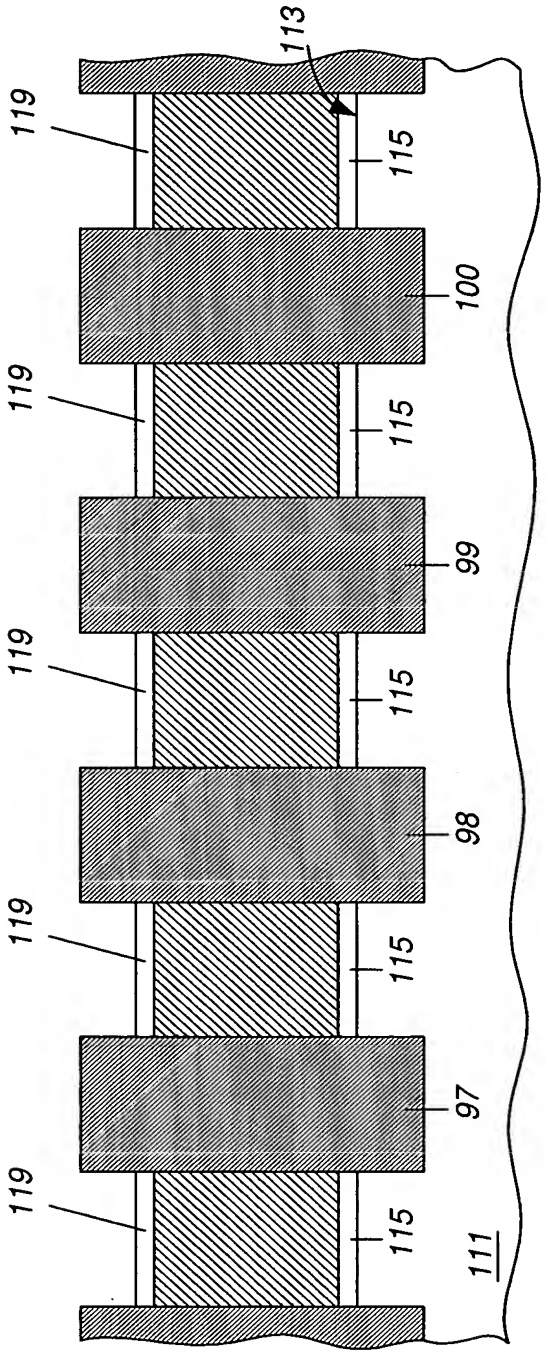



FIG._ 6
(Section B-B)

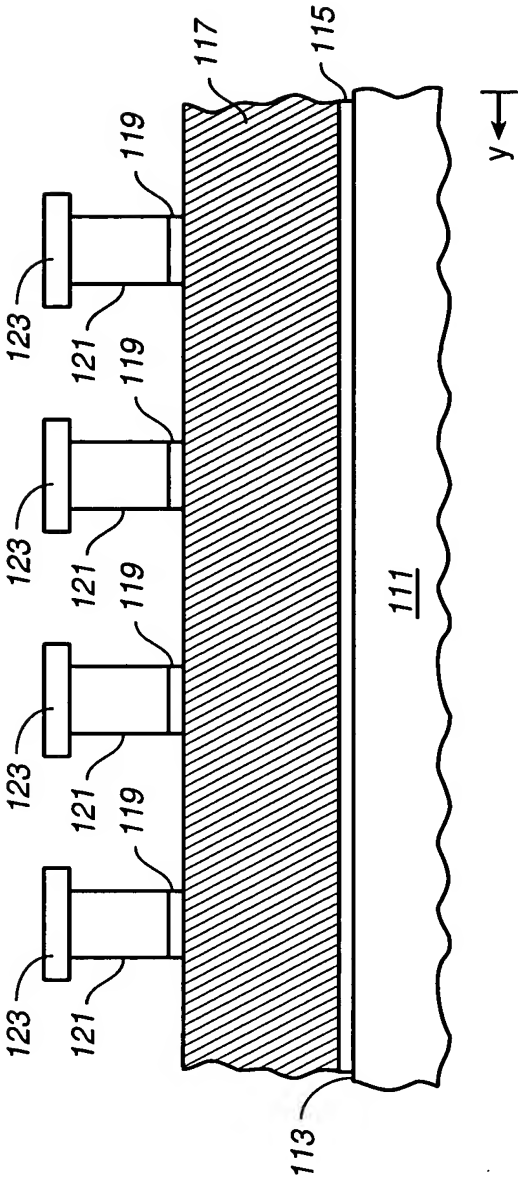

117
115
119
123
121
111
113
y

FIG._7

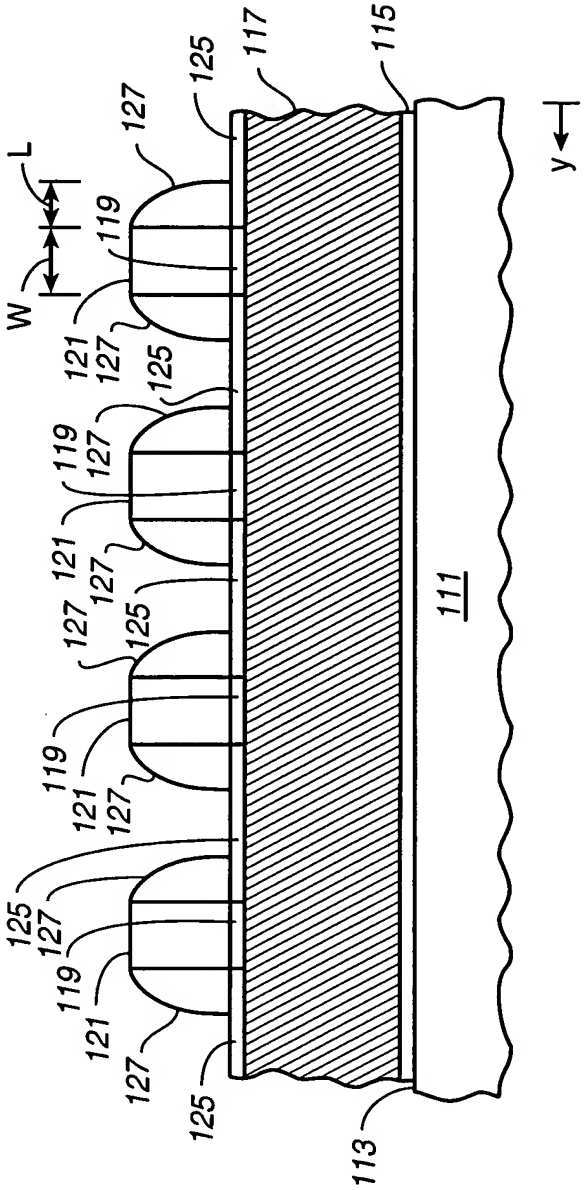

125
117
115
127
L
W
119
121
123
111
113
y

FIG._8

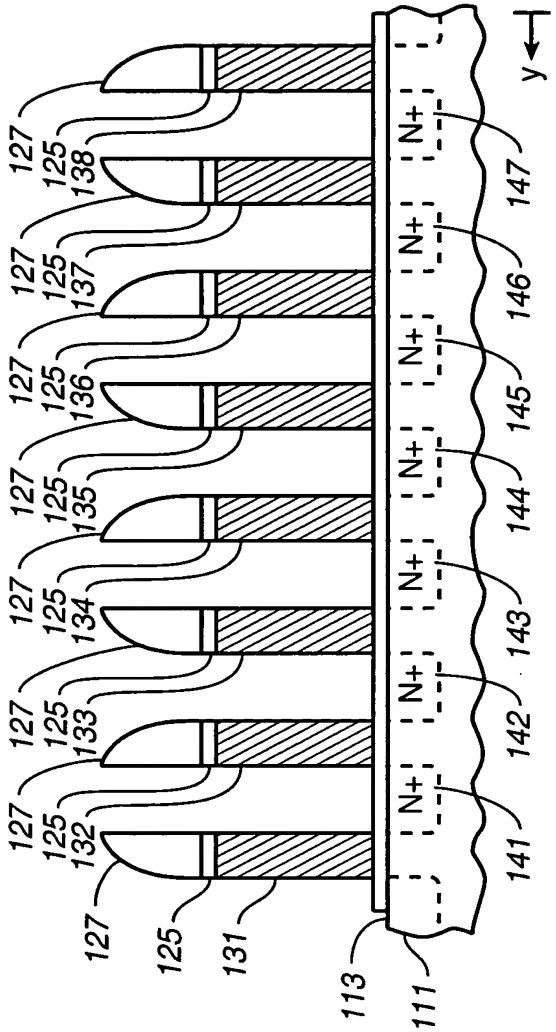

127
125
132
133
134
135
136
137
138
N+
141
142
143
144
145
146
147
111
113
131
y

FIG._9

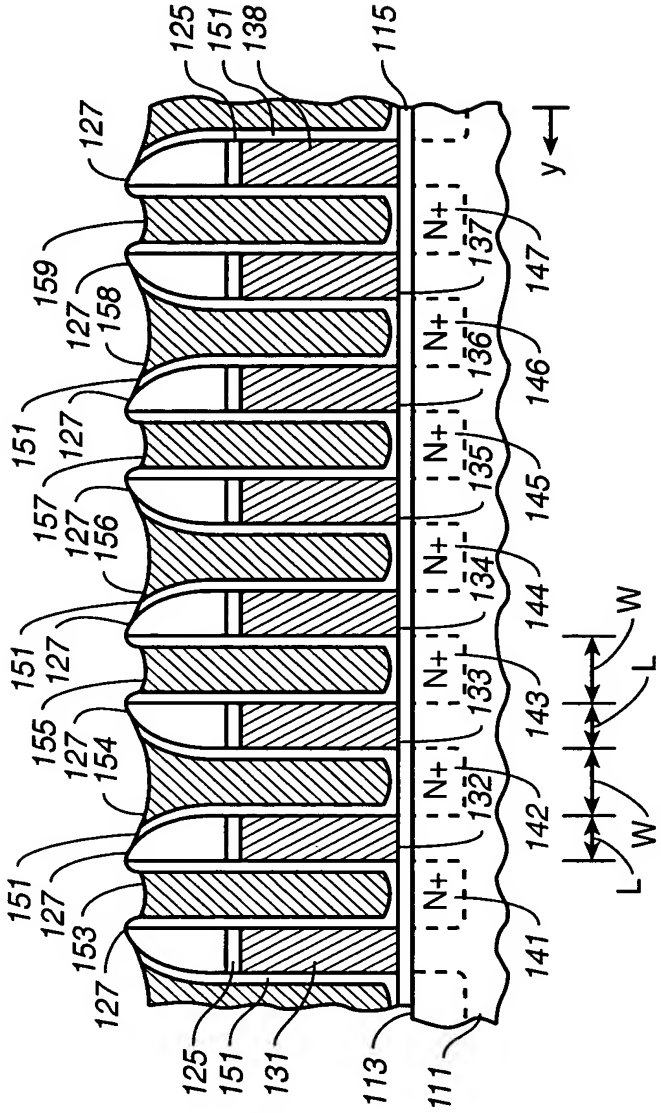

125
151
138
115
127
159
158
157
156
155
154
153
132
133
134
135
136
137
N+
141
142
143
144
145
146
147
111
113
131
y
W
L

FIG._10

FIG._11

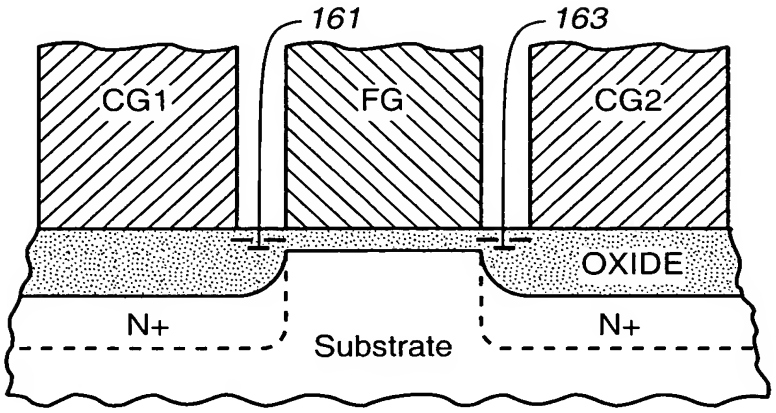



FIG._12

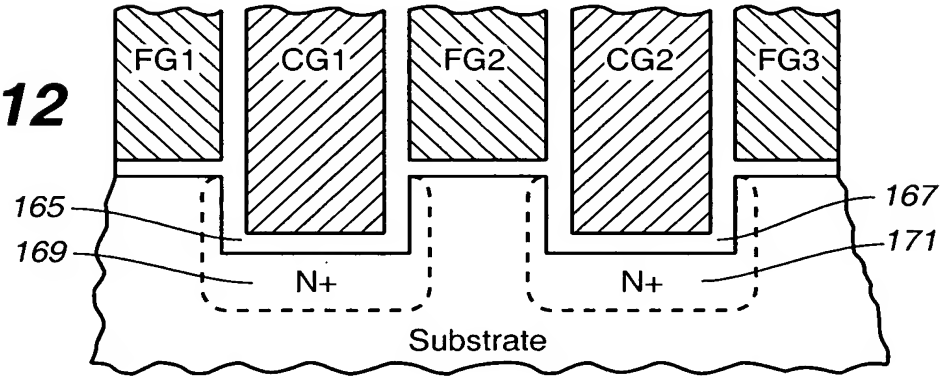
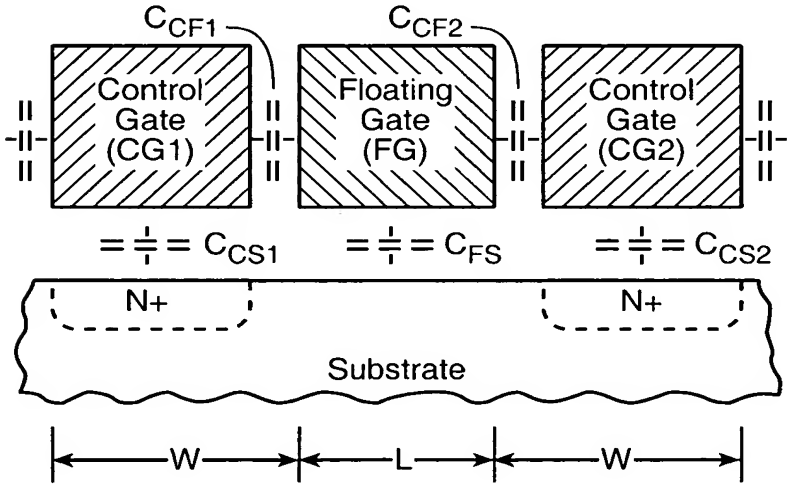



FIG._13



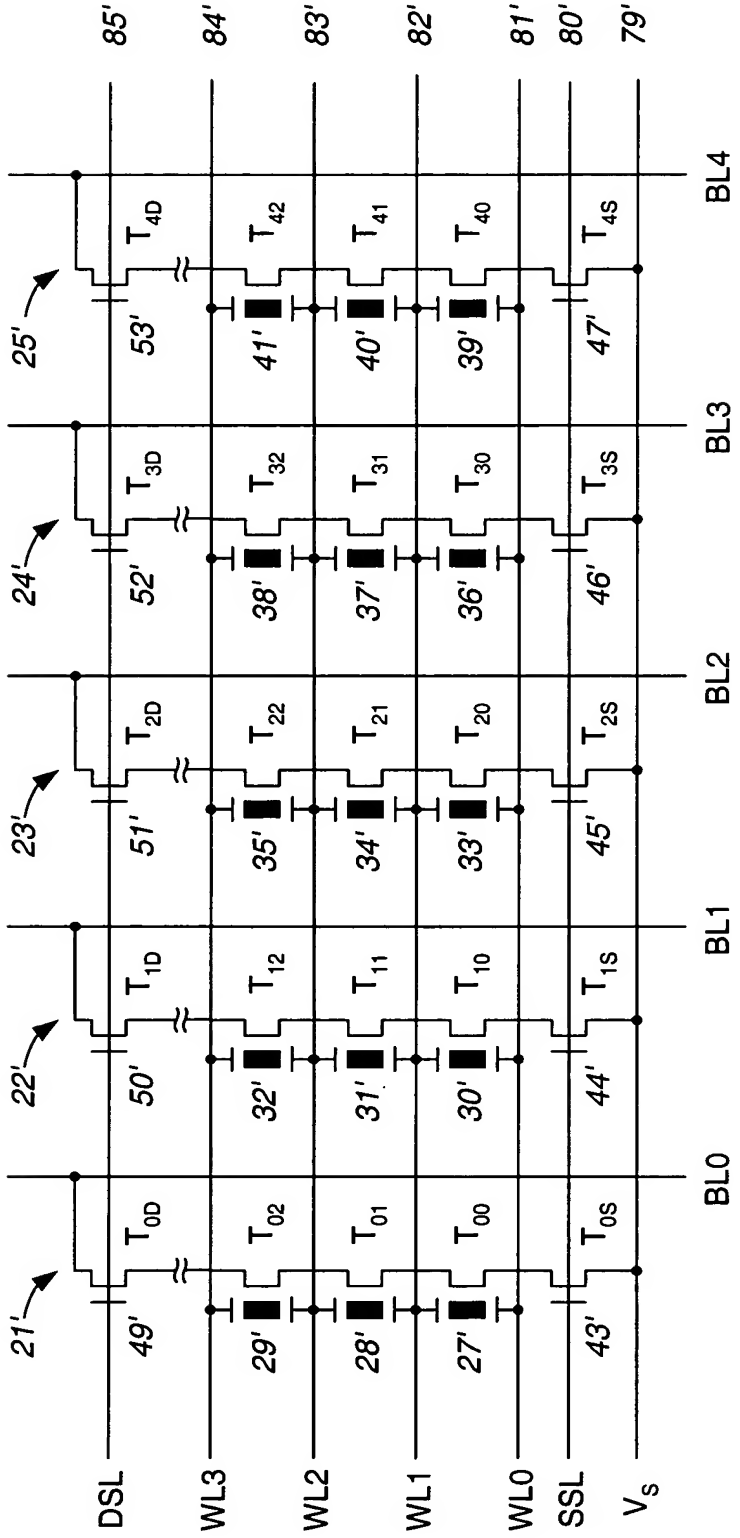

85'
84'
83'
82'
81'
80'
79'
BL4
BL3
BL2
BL1
BL0
25'
24'
23'
22'
21'
$T_{4D}$ $T_{42}$ $T_{41}$ $T_{40}$ $T_{4S}$
$T_{3D}$ $T_{32}$ $T_{31}$ $T_{30}$ $T_{3S}$
$T_{2D}$ $T_{22}$ $T_{21}$ $T_{20}$ $T_{2S}$
$T_{1D}$ $T_{12}$ $T_{11}$ $T_{10}$ $T_{1S}$
$T_{0D}$ $T_{02}$ $T_{01}$ $T_{00}$ $T_{0S}$
53' 41' 40' 39' 47'
52' 38' 37' 36' 46'
51' 35' 34' 33' 45'
50' 32' 31' 30' 44'
49' 29' 28' 27' 43'
DSL
WL3
WL2
WL1
WL0
SSL
$V_S$

FIG._14

| | Erase | Program | Read |
|---|---|---|---|
| $V_D$ (bit lines) | Float | Program: 0v<br>Pgm Inhibit: ~2v | sensed |
| $V_{SSL}$ | Float | ~2v | ~5v |
| $V_S$ | Float | 0 v, Float,<br>or slight positive | 0v |
| P-Well | ~16v | 0 v | 0v |
| $V_{CG}$: (all control gates) | 0v – selected block<br>Float - unselected | - | - |
| Selected cell (both gates) | - | ~13 – 20 v stepped | 0 – 5 v stepped |
| All unselected cells (above selected cell) | - | ~2v | ~5v (1) |
| All unselected cells (below selected cell) | - | ~0v | ~5v (1) |

FIG._15



Appln. No.: Unassigned Docket No.: SNDK.304US1
Title: Flash Memory Cell Arrays Having Dual Control...
Inventors: Harari Exp. Mail: EV321705732US
Filing Date: Herewith Atty. Tel: (415) 318-1160 Sheet 11 of 12

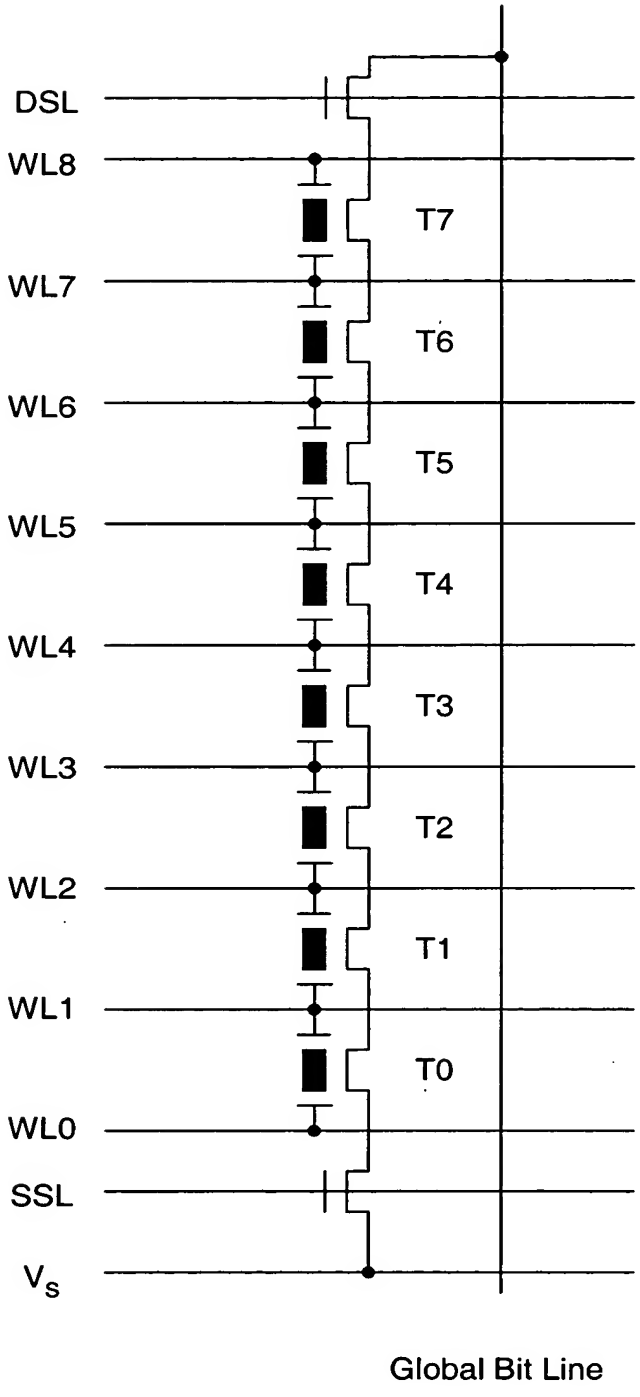

DSL
WL8
T7
WL7
T6
WL6
T5
WL5
T4
WL4
T3
WL3
T2
WL2
T1
WL1
T0
WL0
SSL
$V_S$
Global Bit Line

FIG._16